The claims:

1. A method for fabrication of a semiconductor device on substrate, the semiconductor device having a wafer; the method including the steps:
   (a) applying a seed layer of a thermally conductive metal to a first surface of the wafer;
   (b) electroplating a relatively thick layer of the thermally conductive metal on the seed layer; and
   (c) removing the substrate.

2. A method as claimed in claim 1, wherein the first surface is coated with an adhesion layer prior to application of the seed layer.

3. A method as claimed in claim 1 or claim 2, wherein the seed layer is patterned with photoresist patterns before the electroplating step (b).

4. A method as claimed in claim 3, wherein the electroplating of the relatively thick layer is between the photoresist patterns.

5. A method as claimed in any one of claims 1 to 4, wherein between steps (b) and (c) there is performed the additional step of annealing the wafer to improve adhesion

6. A method as claimed in claim 3 or claim 4, wherein the photoresist patterns are of a height in the range 15 to 500 micrometers.

7. A method as claimed in claim 3 wherein the photoresist patterns have a thickness in the range 3 to 500 micrometers.

8. A method as claimed in any one of claims 3, 4, 6 and 7, wherein the photoresist patterns have a spacing in the range of 200 to 2,000 microns.

9. A method as claimed in any one of claims 1 to 8, wherein the seed layer is electroplated in step (b) without patterning, patterning being performed subsequently.

10. A method as claimed in claim 9, wherein patterning is by photoresist patterning and then wet etching.

11. A method as claimed in claim 9, wherein patterning is by laser beam micro-machining of the relatively thick layer.

12. A method as claimed in any one of claims 3 to 11, wherein the relatively thick layer is of a height no greater that the photoresist height.

13. A method as claimed in any one of claims 3 to 11, wherein the relatively thick layer of thermally conductive metal is electroplated to a height greater than the photoresist and is subsequently thinned.

14. A method as claimed in claim 13, wherein thinning is by polishing or wet etching.

15. A method as claimed in any one of claims 1 to 14, wherein after step (c) there is included an extra step of forming on a second surface of the wafer a second ohmic contact layer, the second ohmic contact layer being selected from the group consisting of: opaque, transparent, and semi-transparent.

16. A method as claimed in claim 15, wherein the second ohmic contact layer is one of blank and patterned.

17. A method as claimed in claim 15 or claim 16, wherein bonding pads are formed on the second ohmic contact layer.

18. A method as claimed in any one of claims 1 to 14, wherein after step (c) ohmic contact formation and subsequent process steps are carried out, the subsequent process steps including deposition of wire bond pads.

19. A method as claimed in claim 18, wherein the exposed second surface is cleaned and etched before the ohmic contact layer is deposited.

20. A method as claimed in any one of claims 15 to 19, wherein the second ohmic contact layer does not cover the whole area of the second surface.

21. A method as claimed in any one of claims 15 to 20, wherein after forming the second ohmic contact layer there is included testing of the semiconductor devices on the wafer.

22. A method as claimed in any one of claims 15 to 21, wherein there is included the step of separating the wafer into individual devices.

23. A method as claimed in any one of claims 1 to 22, wherein the semiconductor devices are fabricated without one or more selected from the group consisting of: lapping, polishing and dicing.

24. A method as claimed in any one of claims 1 to 23, wherein the wafer includes epitaxial layers and, on a first surface of the epitaxial layers remote from the substrate, a first ohmic contact layer; the first ohmic contact layers being on p-type layers of the epitaxial layers.

25. A method as claimed in any claim 22, wherein the second ohmic contact layer is formed on n-type layers of the expitaxial layers.

26. A method as claimed in any one of claims 1 to 14, wherein after step (c), dielectric films are deposited on the epitaxial layers and openings are cut in the dielectric films and second ohmic contact layer and bond pads deposited on the epitaxial layers.

27. A method as claimed in any one of claims 1 to 14, wherein after step (c), electroplating of a thermally conductive metal on the epitaxial layers is performed.

28. A method as claimed in any one of claims 24 to 27, wherein the thermally conductive metal comprises copper and the epitaxial layers comprise multiple GaN-related layers.

29. A semiconductor device comprising epitaxial layers, first ohmic contact layers on a first surface of the epitaxial layers, a relatively thick layer of a thermally conductive metal on the first ohmic contact layer, and a second

ohmic contact layer on a second surface of the epitaxial layers; the relatively thick layer being applied by electroplating.

30. A semiconductor device as claimed in claim 29, wherein there is an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer.

31. A semiconductor device as claimed in claim 30, wherein there is a seed layer of the thermally conductive metal, applied to the adhesive layer.

32. A semiconductor device as claimed in any one of claims 29 to 31, wherein the relatively thick layer is at least 50 micrometers thick.

33. A semiconductor device as claimed in any one of claims 29 to 32, wherein the second ohmic contact layer is a thin layer in the range of from 3 to 500 nanometers.

34. A semiconductor device as claimed in any one of claims 29 to 33, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent.

35. A semiconductor device as claimed in any one of claims 29 to 34, wherein the second ohmic layer includes bonding pads.

36. A semiconductor device as claimed in any one of claims 29 to 35, wherein the thermally conductive metal is copper and the epitaxial layers comprise multiple GaN-related epitaxial layers.

37. A semiconductor device as claimed in any one of claims 29 to 36, wherein the semiconductor device is selected from the group consisting of: a light emitting device, and a transistor device.

38. A semiconductor device comprising epitaxial layers, a first ohmic contact layer on a first surface of the epitaxial layers, an adhesive layer on the first ohmic contact layer, and a seed layer of a thermally conductive metal on the adhesive layer.

39. A semiconductor device as claimed in claim 38, further including a relatively thick layer of the thermally conductive metal on the seed layer, the relatively thick layer acting as a heat sink.

40. A semiconductor device as claimed in claim 38 or claim 39, further including a second ohmic contact layer on a second surface of the epitaxial layers; the second ohmic contact layer being a thin layer in the range of from 3 to 500 nanometers.

41. A semiconductor device as claimed in any one of claims 38 to 40, wherein the second ohmic contact layer comprises bonding pads and is selected from the group consisting of : opaque, transparent, and semi-transparent.

42. A semiconductor device as claimed in any one of claims 38 to 41, wherein the thermally conductive metal comprises copper; and the epitaxial layers comprise GaN-related layers.

43. A method of fabrication of a semiconductor device, the method including the steps:

(a) on a substrate with a wafer comprising multiple GaN-related epitaxial layers, forming a first ohmic contact layer on a first surface of the wafer;

(b) removing the substrate from the wafer; and

(c) forming a second ohmic contact layer on a second surface of the wafer, the second ohmic contact layer having bonding pads formed thereon.

44. A method as claimed in claim 43, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent.

45. A method as claimed in claim 43 or claim 44, wherein the second ohmic contact layer is one of: blank, and patterned.

46. A semiconductor device fabricated by the method of any one of claims 43 to 45.

47. A semiconductor device as claimed in claim 46, wherein the semiconductor device is one of: a light emitting device, and a transistor device.

48. A method for fabrication of a semiconductor device on a substrate, the semiconductor device having wafer with a device layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the wafer remote from the substrate and close to the device layer; and

(b) removing the substrate.

49. A method as claimed in claim 48, wherein the semiconductor device is a silicon-based device.

50. A method for fabrication of a light emitting device on a substrate, the light emitting device having wafer with an active layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the wafer remote from the substrate and close to the active layer; and

(b) removing the substrate.

51. A method as claimed in any one of claims 48 to 50, wherein the thermally conductive layer is as a heat sink.

52. A method as claimed in claim 51, wherein the thermally conductive layer is of a thickness in the range of from 3 microns to 300 microns.

53. A method as claimed in claim 51 or claim 52, wherein the thermally conductive layer is of a thickness of from 50 to 200 microns.